Optimized Hardware Realization of Multiplication Based on Vedic Mathematics Using CBIC

Nouh Asiri, Shuja A. Abbasi and Abdulrahman M. Alamoud

***Abstract*—**Multipliers have become one of the most common components in modern digital Integrated Circuit designs. Vedic Mathematics is the earliest method of Indian mathematics which has a unique technique of calculations based on 16 Formulae. The proposed multiplier technique is from" urdhva tiryakbhayam sutra "which is one of the sutras in Vedic mathematics. Architectures of the proposed Vedic multipliers are implemented on ASIC by using CBIC and state-of-the-art implementation technologies. High-level design techniques are used with the help of advanced EDA tools from SYNOPSYS International. All proposed multipliers are synthesized with Synopsys Design Compiler through saed32lvt_ss0p95vn40c library file. The performance of the proposed multiplier was examined and compared to well-known multipliers such as Traditional Wallace Multiplier, Reduced Complexity Wallace multiplier and Dadda multiplier. It is demonstrated that the proposed multiplier is superior in terms of speed as well as power consumption, and showed minimum size for multiplication of various bits-lengths.

***Keywords*—** Multiplier, Vedic Mathematics, Design Compiler, CBIC

I. Introduction

Addition subtraction, Multiplication and division are the principal functions included in Arithmetic operations. The one which is frequently used in arithmetic is Multiplication [1]. Multiplication is commonly used in the main blocks which are Arithmetic logical unit and multiply besides accumulate MAC in Digital Signal Processing (DSP) applications. DSP applications are implemented in Fast Fourier Transform (FFT) and microprocessors [2]. Multipliers with high speed are required in DSP processors to reduce the time of execution. At present, the time of execution for digital signal processing chip relies upon the time of multiplication. The high speed processors are most required recently as a result of the technology advancement in various applications of DSP [3]. A number of multipliers, demonstrating several advantages, have been reported in the last few decades.

There is a good deal of multiplier techniques used by many researchers for ASIC based multiplication, such as multiplication with Wallace tree adders [4]–[5], with carry save adders (CSA) [6]–[9], multiplication based on booth approach [10]–[12] and Booth-Wallace tree multiplier [13]. The multipliers created with the aforementioned approaches and techniques lack speed and also occupy large area and waste significant amount of power when implemented on ASIC.

Further, besides speed and power issues in selecting an algorithm to design a multiplier, technology implementation is becoming the next issue. Every ASIC manufacturer could create functional blocks with known electrical characteristics, such as propagation delay, capacitance and inductance. Standard-cell design, also known as Cell Based IC (CBIC) is the utilization of these functional blocks to achieve very high gate density and good electrical performance. The CBIC designer defines only the placement of the standard cells and the interconnect. The use of predesigned, tested, and characterized standard-cell library gives the advantage of drastic reduction in design time and money, and reduced risk. In addition each standard cell can be optimized individually [14]–[15].

In the present work, an attempt is made to design a multiplier based on Vedic mathematics and implement it using CBIC technology.

II. Proposed Multiplier

The present work is based upon the Vedic multiplier techniques. A brief account of this is given below:

A. Vedic Mathematics

Vedic mathematics has its roots in the Vedas, which are ancient Indian texts first written in Sanskrit and thought to have originated around 2000 BC. Spiritual leader and mathematician, Sri Bharati Krsna Tirthaji reconstructed 16 sutras, or fundamental principles, derived from these ancient texts. The sutras, along with 13 sub-sutras, are the basis for the Vedic mathematics system [16]. Vedic multiplication is an efficient and simple form of mental calculation. One of the "sutras" or "formulas" in Vedic mathematics is "Urdhva-tiryakbhyam" meaning vertically and crosswise.

To illustrate this multiplication scheme, let us consider the multiplication of two decimal numbers (5498 × 2314). The conventional methods already known to us will require 16 multiplications and 15 additions. An alternative method of multiplication using Urdhva tiryakbhyam Sutra is shown in Figure 1. The numbers to be multiplied are written on two consecutive sides of the square as shown in the figure. The square is divided into rows and columns where each row/column corresponds to one of the digit of either a

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multiplier or a multiplicand. Thus, each digit of the multiplier has a small box common to a digit of the multiplicand. These small boxes are partitioned into two halves by the crosswise lines. Each digit of the multiplier is then independently multiplied with every digit of the multiplicand and the two-digit product is written in the common box. All the digits lying on a crosswise dotted line are added to the previous carry. The least significant digit of the obtained number acts as the result digit and the rest as the carry for the next step. Carry for the first step (i.e., the dotted line on the extreme right side) is taken to be zero [17].

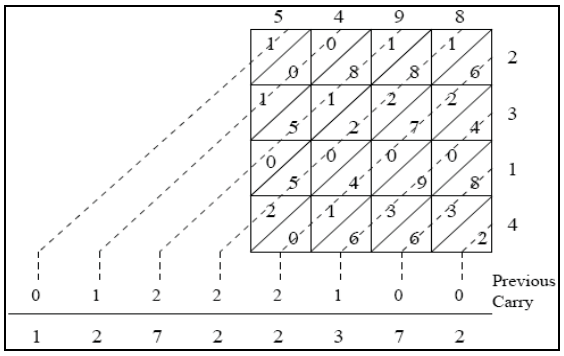


Fig. 1 Alternative way of multiplication by Urdhva tiryakbhyam Sutra

B. *The 2x2 bit Vedic multiplier module*

The 2X2 Vedic multiplier module is implemented using four input AND gates & two half-adders which is displayed in its block diagram in Figure 2. It is found that the hardware architecture of 2x2 bit Vedic multiplier is same as the hardware architecture of 2x2 bit conventional Array Multiplier [18]. Thus the multiplication of 2 bit binary numbers by Vedic method does not make significant effect in improvement of the multiplier"s efficiency. Very precisely we can state that the total delay is only 2-half adder delays, after final bit products are generated, which is very similar to Array multiplier. So we switch over to the implementation of 4x4 bit Vedic multiplier which uses the 2x2 bit multiplier as a basic building block.

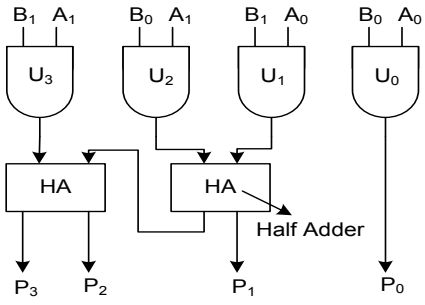


Fig. 2 A schematic circuit of 2x2 multipliers

C. *The 4x4 bit Vedic multiplier module*

The 4x4 bit Vedic multiplier module is implemented using four 2x2 bit Vedic multiplier modules as discussed in Figure 3. Analyzing 4x4 multiplications, say A= A3 A2 A1 A0 and B= B3 B2 B1 B0, the output line for the multiplication result is = P7 P6 P5 P4 P3 P2 P1 P0. Let's divide A and B into two parts, say A3 A2 & A1 A0 for A and B3 B2 & B1 B0 for B. Using the fundamentals of Vedic multiplication, taking two bits at a time and using 2 bit multiplier block, we can have the structure for multiplication as shown in Figure 3.

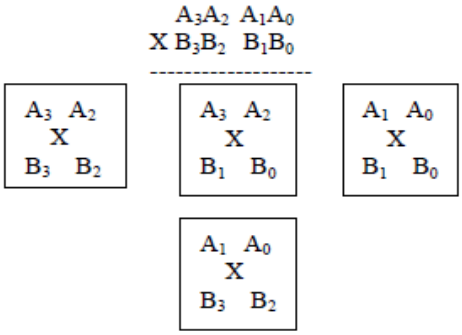


Fig. 3 Block diagram of 4x4 multiplications

Each block as shown above is 2x2 bit Vedic multiplier. First 2x2 bit multiplier inputs are A1 A0 and B1 B0. The last block is 2x2 bit multiplier with inputs A3 A2 and B3 B2. The middle one shows two 2x2 bit multiplier with inputs A3 A2 & B1 B0 and A1 A0 & B3 B2. So the final result of multiplication, which is of 8 bit, P7 P6 P5 P4 P3 P2 P1 P0. To understand the concept, the Block diagram of 4x4 bit Vedic multiplier is shown in Figure 4. To get final product (P7 P6 P5 P4 P3 P2 P1 P0), four 2x2 bit Vedic multiplier (Figure 2) and three 4-bit Ripple-Carry (RC) Adders are required.

The same method can be extended for input bits 8, 16, 32 and 64. However, first the basic blocks, i.e. the 2x2 bit multipliers are made and then, using these blocks, 4x4 multipliers are designed by adding the partial products using Ripple carry adders. The 4x4 blocks are then used to design 8x8 blocks and so on. The block diagram for 4x4 bit multiplier is shown in Figure 4.

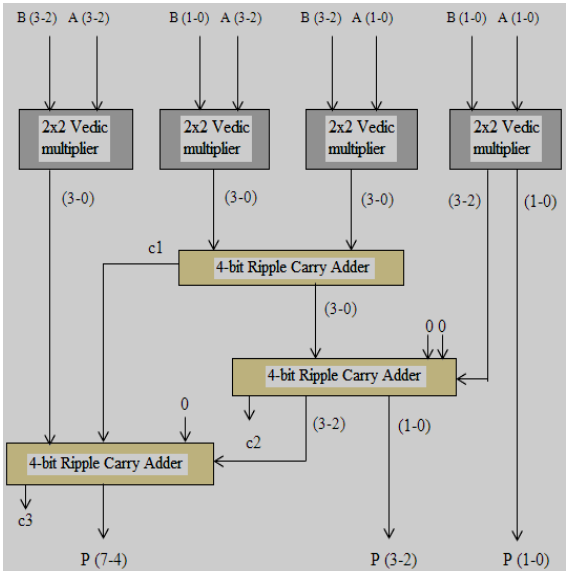


Fig. 4 Block diagram of a 4x4 multiplier

III. Results And Discussion

In this section we show results for the 8x8, 16x16, 32x32 and 64x64 Vedic multipliers, synthesized with Synopsys Design Compiler using saed32lvt_ss0p95vn40c library file.

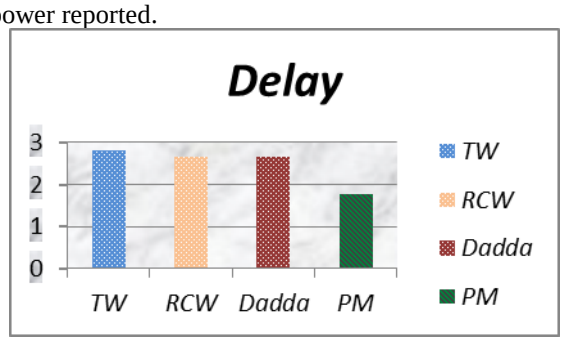
The performances of the multipliers are compared on the basis of area, delay and power consumed. The results will be presented in table 1. In addition, comparisons with earlier reported multipliers like Traditional Wallace(TW) Multiplier, Reduced Complexity Wallace multiplier (RCW) and Dadda multiplier) [19] are done to show the superiority of the proposed multipliers (PM).

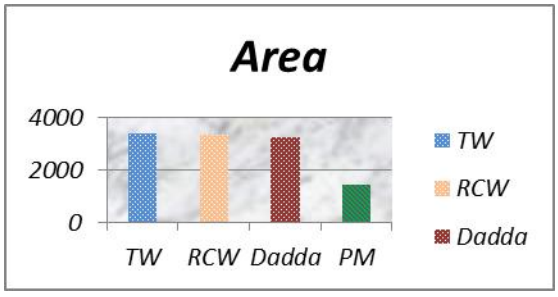
TABLE I
DELAY, AREA AND POWER OF THE PROPOSED MULTIPLIERS AND OTHER REPORTED MULTIPLIERS

Size	Delay (ns)			
	PM	Dadda	RCW	TW
8x8	1.76	2.64	2.64	2.8
16x16	2.96	3.8	3.65	4.13
32x32	5.48	14.82	14.62	14.83
64x64	9.75	21.98	21.54	22.88
Area (μm^2)				
8x8	1432.25	3262	3346	3392
16x16	6398.01	14242	14372	14847
32x32	28026.54	59086	59271	61526
64x64	121342.9	238597	238843	246842
Power *(mw)*				
8x8	0.2216	1.94	2.04	1.92
16x16	1.11	11.22	11.41	11.09
32x32	5.3348	53.11	52.74	51.85
64x64	25.645	222.64	219.17	216.50

A. 8x8Multiplier Results

A comparison of the results (Delay, Area, Power) of the 8-bit proposed multiplier with some types of multipliers reported in [19] is given in the table.1 and Figure 5. From the results, it is found that the proposed multiplier, has the lowest delay, which is 1.76 ns. This delay is almost one third of Multiplier (TW, RCW and Dadda) reported and the area is less by (57%) of these Multipliers. The proposed 8-bit multiplier consumes total power at about 0.2216 mw or around 90% less than the total power reported.





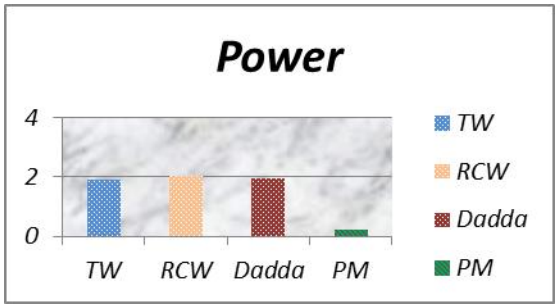
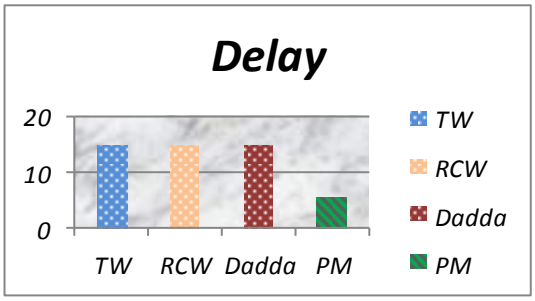
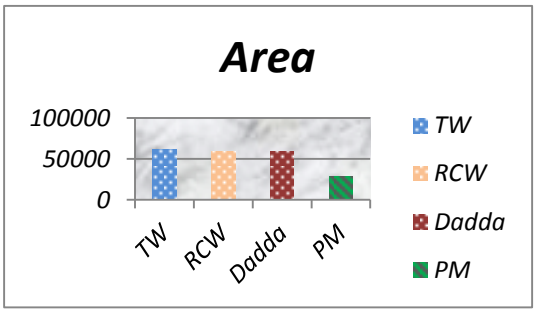


Fig. 5 Delay, Area and Power comparison of 8-bit multipliers

B. 32x32 Multiplier Results

When the bit-length of a multiplier is increased, for example, in the case (TW) multiplier the delay increases from 4.13 ns for 16-bit to 14.83 ns for 32-bit, the delay increases more than three times. In contrast, only a small increase in delay is found in the 32-bit proposed Multiplier (PM), which is 3.08 ns for 16-bit to 5.49 ns for 32-bit - less than double. This trend can be seen in Figure 6. The proposed multiplier still maintains its superiority and achieves best performance in the cases of area and total power, as shown in the table 1. and Figures 6.





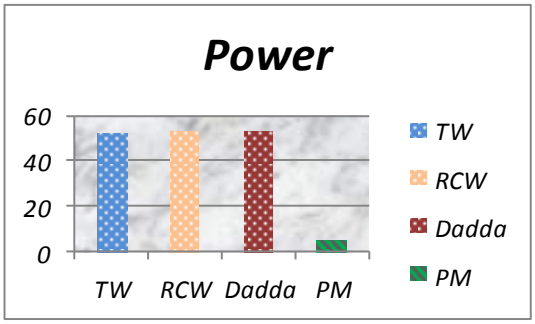


Fig. 6 Delay, Area and Power comparison of 32-bit multipliers

IV. Conclusion

This paper presents a highly efficient method of multiplication –"Urdhva Tiryakbhyam Sutra" based on Vedic mathematics. The architectures of 8x8 bits, 16x16 bits, 32x32 bits and 64x64 bits Vedic multipliers are proposed and designed in ASIC technology. The performance of the proposed multipliers using Vedic Sutra proved to be efficient in terms of speed, area and power. As the input bits increases, relatively the efficiency of the circuit is also increases. The main advantage is delay increases slowly as input bits increase. It is also demonstrated that this design is quite efficient in terms of silicon area/speed. The proposed Vedic multipliers architecture shows good improvement in power consumption. There multipliers can be efficiently used in any DSP application or in any DSP processors that requires low power consumption.

Acknowledgment

This project was supported by NSTIP strategic technologies programs, number (11_NAN-2118-02) in the Kingdom of Saudi Arabia.

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